Amendments to the Claims

A complete list of pending claims follows, with indicated amendments:

1. (Currently Amended) An information handling system having a multi-host virtual bridge input-output resource switch, said system comprising:

a plurality of server modules, each of said plurality of server modules having at least one central processing unit (CPU), memory and at least one server input-output (I/O) port;

a plurality of input-output (I/O) modules, each of said plurality of input-output modules having a module I/O port adapted for coupling to any one of the at least one server I/O port; and

at least one input-output (I/O) switch comprising:

a plurality of input buffers, wherein a one of the plurality of input buffers is coupled to each of the at least one server I/O port of each of the plurality of server modules and another one of the plurality of input buffers is coupled to the module I/O port of each of the plurality of I/O modules;

a plurality of output buffers, wherein a one of the plurality of output buffers is coupled to each of the at least one server I/O port of each one of the plurality of server modules and another one of the plurality of output buffers is coupled to the module I/O port of each of the plurality of I/O modules;

a plurality of multiplexers, wherein said plurality of input buffers and said plurality of output buffers are coupled to said plurality of multiplexers; and

control logic for controlling said plurality of multiplexers, wherein said plurality of multiplexers determine which ones of said plurality of input buffers

are coupled to which ones of said plurality of output buffers;

said at least one I/O switch is coupled to each of the at least one server I/O ports and to each of the module I/O ports, wherein said at least one I/O switch statically couples selected ones of the at least one server I/O ports to selected ones of the module I/O ports so that each of the plurality of server modules will boot its operating system and recognize the statically coupled ones of the module I/O ports.

2. (Original) The information handling system according to claim 1, further comprising a bridge for coupling the CPU to the memory and to the at least one server I/O port.

3. (Original) The information handling system according to claim 1, further comprising at least one native input-output (I/O) device in at least one of said plurality of server modules.

4. (Previously Presented) The information handling system according to claim 3, wherein the at least one native I/O device is an interface selected from the group consisting of USB, serial, keyboard, video and mouse interfaces.

5. (Original) The information handling system according to claim 1, further comprising an Ethernet controller in at least one of said plurality of server modules.

6. (Original) The information handling system according to claim 1, wherein the at least one server I/O port is a serial port.

7. (Original) The information handling system according to claim 1, wherein the module I/O port is a serial port.

8. (Original) The information handling system according to claim 1, wherein the at least one server I/O port is a serial PCI I/O port.

9. (Original) The information handling system according to claim 1, wherein the module I/O port is a serial PCI I/O port.

10-11. (Previously Canceled)

12. (Previously Presented) The information handling system according to claim 1, further comprising a mapping table coupled to said control logic, said mapping table storing which ones of said plurality of input buffers are coupled to which ones of said plurality of output buffers.

13. (Original: The information handling system according to claim 12, further comprising initialization logic for initializing said control logic and said mapping table.

14. (Original) The information handling system according to claim 13, wherein said initialization logic is external from said at least one I/O switch.

15. (Original) The information handling system according to claim 14, wherein said initialization logic is coupled to said control logic with a low pin count interface.

16. (Original) The information handling system according to claim 15, wherein the low pin count interface is selected from the group consisting of I^2C and JTAG.

17. (Original) The information handling system according to claim 1, wherein said at least one I/O switch is accessed through a user interface.

18-27. (Previously Canceled)